Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled).

2. (Currently Amended) A plating method for a printed circuit board, comprising:

providing a substrate having a plurality of connection pads and a plurality of circuit patterns connected to the plurality of connection pads;

using ~~some~~a first set of the plurality of circuit patterns provided in the substrate as a first power connection portion and ~~some~~a second set of the plurality of circuit patterns, separate from the first set, as a second power connection portion, and ~~selectively~~ connecting one of the first or second power connection portion to an external power source;

covering a surface of the substrate excepting the connection pads with a plating resistance resist to shield it;

selectively supplying power to the one of the first or the second power connection portion, and forming a gold-plated layer on a connection pad to which the one of the first or the second power connection portion is electrically connected; ~~and~~

disconnecting the one of the first or the second power connection portion from the external power source; and

connecting the other of the first or second power connection portion to an external power source, wherein using ~~some~~ the first set of the plurality of circuit patterns provided in the substrate as a first power connection portion and ~~some~~ the second set of the plurality of circuit patterns as a second power connection portion~~, and selectively connecting the first or the second power connection portion to the external power source~~ comprises:

coating a photoresist at the surface of the substrate;

removing a portion of the photoresist to expose a connection pad and exposing some of the circuit patterns to form ~~a~~the first power connection portion;

coating a conductive layer on the surface of the substrate ~~for connecting~~to form a connection between the first power connection portion and the external power source; and

repeating the coating, removing and coating steps to form ~~a~~the second power connection portion.

3. (Previously Presented) The method of claim 2, wherein the first and second power connection portions are formed by removing a photoresist from corresponding portions of the circuit pattern, and receive power by being connected to the conductive layer.

4. (Previously Presented) The method of claim 2, wherein the conductive layer is formed through an electroless plating method.

5. (Previously Presented) The method of claim 2, wherein the conductive layer has a thickness of 0.3~0.7 μm.

6. (Previously Presented) The method of claim 2, wherein the conductive layer is formed to have a desired thickness by additionally performing an electrolytic plating method on the formed conductive layer.

7. (Previously Presented) The method of claim 2, wherein the plating resistance resist is coated on the surface of the substrate formed with the conductive layer.

8. (Previously Presented) The method of claim 2, wherein disconnecting the one of the first or the second power connection portion from the external power source comprises:

removing the conductive layer and the plating resistance resist; and

coating a photoresist on the surface of the conductive layer and the plating resistance resist-removed substrate to cover the one of the first or the second power connection portion.

9. (Previously Presented) A plating method for a printed circuit board, comprising:

providing a substrate having a plurality of bonding pads and ball pads at both sides thereof and a circuit pattern to which the bonding pads and the ball pads are connected;

using some of the circuit patterns provided at the surface of the substrate as first and second power connection portions and connecting the first power connection portion to an external power source;

covering the surface of the substrate having the ball pad formed thereon with a plating resistance resist to shield it;

supplying power to the bonding pad through the first power connection portion for forming a gold-plated layer on the bonding pad;

removing the connection from the external power source to the first power connection portion;

connecting the second power connection portion to the external power source and coating a plating resistance resist at the surface of the substrate with the bonding pad formed thereon to shield it;

supplying power to the ball pad through the second power connection portion for forming a gold-plated layer on the ball pad; and

removing the connection from the external power source to the second power connection portion.

10. (Previously Presented) The method of claim 9, wherein the using some of the circuit patterns provided at the surface of the substrate as first and second power connection

portions and connecting the first power connection portion to the external power source comprises:

coating a photoresist on both surfaces of the substrate;

removing a portion of the photoresist to expose the bonding pad and the ball pad and exposing some of the circuit patterns to form each of the first and second connection portion; and

coating a conductive layer on the surface of the substrate where the ball pad is formed in order to connect the first power connection portion to the external power source.

11. (Previously Presented) The method of claim 10, wherein the first and second power connection portion is formed by removing a photoresist from a portion of the circuit pattern, and receives power by being connected to the conductive layer.

12. (Previously Presented) The method of claim 10, wherein the conductive layer is formed through an electroless plating method.

13. (Previously Presented) The method of claim 10, wherein the conductive layer has a thickness of approximately 0.3~0.7 μm.

14. (Previously Presented) The method of claim 10, wherein the conductive layer is formed to have a desired thickness by additionally performing an electrolytic plating method on the formed conductive layer.

15. (Previously Presented) The method of claim 10, wherein the plating resistance resist is coated on the surface of the substrate with the conductive layer formed thereon.

16. (Previously Presented) The method of claim 10, wherein the removing the connection from the external power source to the first power connection portion comprises :

removing the conductive layer and the plating resistance resist; and

coating a photoresist at the surface of the conductive layer and the plating resistance resists-removed substrate to cover and insulate the power connection portion in the substrate.

17. (Previously Presented) The method of claim 9, wherein the connecting the second power connection portion to the external power source and coating the plating resistance resist at the surface of the substrate with the bonding pad formed thereon to shield it comprises:

forming a conductive layer at the surface of the substrate where the bonding pad is formed to electrically connect it to the second power connection portion; and

coating a plating resistance resist on a surface of the conductive layer.

18. (Previously Presented) The method of claim 10, wherein the removing the connection from the external power source to the second power connection portion comprises:

removing the plating resistance resist and the conductive layer; and

covering the second power connection portion with a photoresist to make the second power connection to be insulated in the substrate.

19. (Currently Amended) A plating method for a printed circuit board comprising:

providing a substrate having a plurality of connection pads and circuit patterns connected to the connection pads;

using some of the circuit patterns provided in the substrate as a first power connection portion and some of the circuit patterns as a second connection portion, and ~~selectively~~ connecting one of the first or the second power connection portion to an external power source;

covering a surface of the substrate excepting the connection pads with a plating resistance resist to shield it;

~~selectively~~ supplying power to the one of the first or the second power connection portion and forming a gold-plated layer on a connection pad to which the one of the first or the second power connection portion is electrically connected; ~~and~~

disconnecting the one of the first or the second power connection portion from the external power source, comprising:

removing the plating resistance resist; and

coating a photoresist on the surface of the plating resistance resist-removed substrate to cover and insulate the one of the first or the second power connection portion in the substrate; and

connecting the other of the first or second power connection portion to the external power source.